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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional): 10030549-1

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)]

on 2010-06-15

Signature /Gregory W. Osterloth/

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Application Number	Filed
10/681,068	2003-10-07

First Named Inventor: Andrew S. Hildebrant, et al.

Art Unit	Examiner
3714	Frank M. Leiva

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- ☐ applicant/inventor.
- ☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- ☑ attorney or agent of record. Registration number 36,232.
- ☐ attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____

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2010-06-15
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NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	:	10/681,068	Confirmation No. : 8619
Applicant	:	Andrew S. Hildebrant, et al.	
Filed	:	10/7/2003	
TC/A.U.	:	3714	
Examiner	:	Frank M. Leiva	
Docket No.	:	10030549-1	

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRE-APPEAL BRIEF

Sir:

This Pre-Appeal Brief is submitted in response to the Final Office Action mailed March 15, 2010.

Claims 1-17 remain in the application, all of which stand rejected.

1. Rejection of Claims 1-5 and 7-16 Under 35 USC 102(b)

Claims 1-5 and 7-16 stand rejected under 35 USC 102(b) as being anticipated by Agrawal (US 5,257,268).

Claim 1 recites:

1. A machine-executable method comprising:
executing sequences of instructions on a machine, the executed sequences of instructions causing the machine to perform the actions of,
reading a test file having a plurality of test vectors;
determining a required memory needed to execute the plurality of test vectors; and

using the required memory to estimate a cost to execute the test vectors.

With respect to claim 1, the Examiner asserts that Agrawal discloses "determining a required memory needed to execute [a] plurality of test vectors" in col. 4:40-60, where Agrawal discloses a system that determines "the minimum required number of flip-flops gates (memory)". *See*, 3/15/2010 Final Office Action, p. 4. Applicants respectfully disagree.

Agrawal discloses that:

> . . .A sequential circuit. . .is fully initialized when all its memory elements are in known states. One has to provide a set of initialization vectors to bring a circuit to a known state, and those initialization vectors must be chosen appropriately. In accordance with our preferred embodiment, the initialization vectors are generated by a procedure that minimizes a "cost function". We chose our cost function to correspond to the number of flip-flops in the "unknown" state, but other cost functions are also possible.
>
> As shown in the flow chart of FIG. 2, the initialization process begins at block 100 with the assumption that all flip-flops are at the "unknown" state, and the cost function is simply equal to the number of flip-flops in the circuit, M. The process of selecting a set of initialization vectors consists of generating "trial vectors" and accepting only those trial vectors that reduce the cost.

Col. 4, lines 43-60.

From the above excerpt, applicants believe it is clear that Agrawal does not disclose an action of "determining a required memory needed to execute [a] plurality of test vectors", as the Examiner asserts. Instead, Agrawal discloses how to determine what vectors are needed to initialize the flip-flops of a circuit under test. Agrawal does this by first setting up a cost function and initializing it to some value, such as the number of flip-flops in the circuit that are in an unknown state. AFTER setting up the cost function, Agrawal generates or selects a "trial vector", and simulates its application to the circuit to be tested. After application of the trial vector to the circuit, Agrawal counts the number of flip-flops that remain in an unknown state and compares this count to the value of the cost function. If the value of the cost function (i.e., the "total cost") is

reduced, the trial vector is saved as an initialization vector, and a different trial vector is selected or generated and applied to the circuit. Only those trial vectors that reduce the value of the cost function are added to the set of initialization vectors. When the cost function reaches zero, or falls below some preset threshold, the set of initialization vectors is deemed complete. *See*, e.g., Agrawal's FIG. 2 and col. 4:61 - 5:68.

Of note, Agrawal never determines the "required memory needed to execute" the set of initialization vectors. Rather, Agrawal applies each of a number of trial vectors to a circuit (without determining a required memory needed to execute any of the trial vectors), and after each application makes a determination of how many flip-flops remain in an unknown state (again, without determining a required memory needed to execute any of the trial vectors). Agrawal's application of trial vectors, and iterative assessment of the number of flip-flops remaining in an unknown state, continues until the number of flip-flops remaining in an unknown state falls below a certain value (or is equal to zero). However, Agrawal never determines a required memory needed to execute the trial vectors (or even one of the trial vectors). Instead, Agrawal determines a required number of trial vectors to initialize a fixed number of flip-flops in a circuit.

Given that Agrawal does not disclose "determining a required memory needed to execute the plurality of test vectors", it follows that Agrawal cannot disclose "using the required memory to estimate a cost to execute the test vectors." In particular, the "cost function" disclosed by Agrawal is not "a cost to execute. . .[a plurality of] test vectors". Instead, Agrawal's "cost function" is an optimization function that is used to limit growth in a set of initialization vectors. For example, in a simple case, an initialization vector is not added unless it actually causes additional flip-flops to be initialized optimum number of initialization vectors.

Because Agrawal does not disclose each and every recitation of applicants' claim 1, applicants believe the Examiner has committed clear error, and claim 1 is believed to be allowable.

Claims 2-5 and 7 are believed to be allowable, at least, because they depend from claim 1.

Claims 8-16 are believed to be allowable, at least, for reasons similar to why claim 1 is believed to be allowable.

2. Rejection of Claims 6 and 17 Under 35 USC 103(a)

Claims 6 and 17 stand rejected under 35 USC 103(a) as being unpatentable over Agrawal.

Applicants' claims 6 and 17 are believed to be allowable, at least, because they respectively depend from claims 1 and 13.

3. Conclusion

Given the above arguments and remarks, applicants respectfully request the issuance of a Notice of Allowance.

Respectfully submitted,
HOLLAND & HART, LLP

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